Technical document

This technical document describes the specifications and technical skills required to the packaging companies participating in the agreement.

Technical notes and glossary of terms

Channels: The number of single SiPM or a group of SiPM which should be individually readable from the package (the number of independent outputs of the device).

SiPM: Silicon photomultipliers, silicon solid state photo-detector

CSP: Chip scale package is type of integrated circuit package in which the silicon/semiconductor die is mounted on a PCB/interposer. The package must not have an area much greater than that of the die and it must be a single-die, direct surface mountable package.

SMD: Surface-mount devices, i.e. a component which can be directly mounted onto the surface of a printed circuit board.

Through-hole: The components are inserted into holes drilled in printed circuit boards (PCB) and soldered to pads on the opposite side either by manual assembly (hand placement) or by the use of automated insertion mount machines.

Array/Tile: A device composed of multiple channels, usually *Array* refers to a device containing 1xN channels whereas *Tile* refers to a device of MxN channels (M,N>1).

Production quantities: since devices can have a very different number of channels (from 1 up to several hundreds) the term quantities usually refers to the total number of channels required for a production (number of devices x number of channel per device).

Mini production: < 1000 channels

Pre series: 1000< channels<10000

Full volume production: > 10000 channels

Required specifications and skills

In order to participate in the agreement, the company have to provide a list of the machines / facilities available, the average numbers for production per year and the average timing for production.

In addition, the following skills are required:

• Processing of ceramic substrates with screen printing and laser marking techniques.

• Removal of impurities and contaminants from the substrate surface with plasma cleaning technique.

• Automatic die placing with conductive and non-conductive die attach, with sorting and extraction of devices from 6 " or 8 " wafers on tape or waffle pack.

• Automatic wire bonding with 17 and 25um gold wire, ball and wedge bonding with the possibility of deep access.

• Deposition of epoxy and silicon resins with the possibility of varying the thickness of the resin and the application technique, in the absence or presence of vacuum and at a controlled temperature, including direct pouring technique and mold resin technique.

• Possibility of integrating cooling circuits into ceramic substrates.

• Positioning tolerances, PCB size, milling in the order of 100um.

Examples

Below are some examples of projects developed in FBK, useful for packaging companies to evaluate the feasibility of future projects.

Example project 1

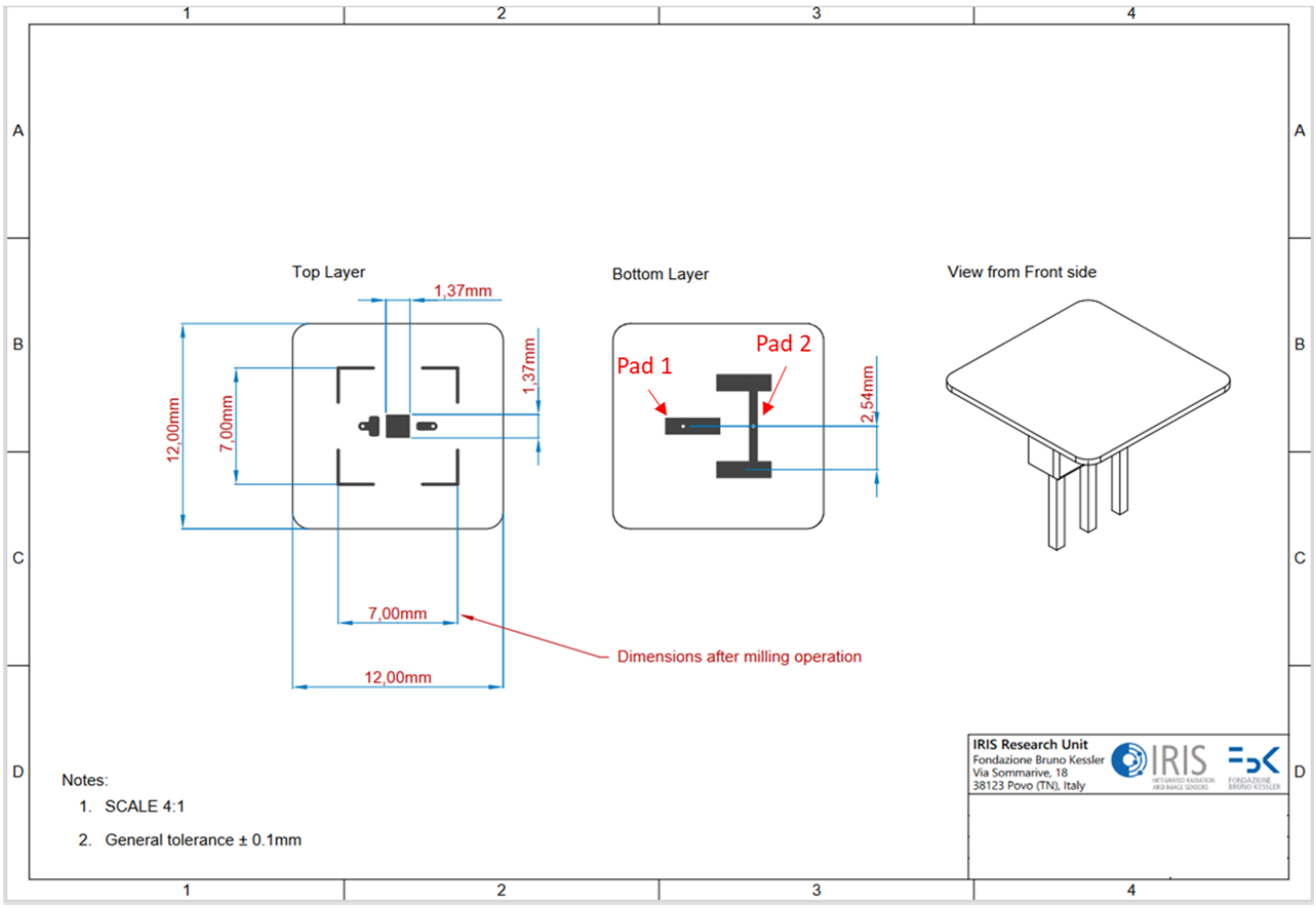
Packaging of 1x1mm SiPM mounted with conductive resin on a PCB 12mmx12mm. The SiPM pads are wire bonded on the PCB pads with wedge or ball bonding and 3 pin (2.54mm-pin pitch) are electrically connected with the PCB pads on the bottom side, in the following way:

Central pin = Pad 1

Left and right pins = Pad 2

No optical resin is used to encapsulate the SiPM, thus touching the SiPM surface and/or the bonding can induce a damage on the device and affect the performance.

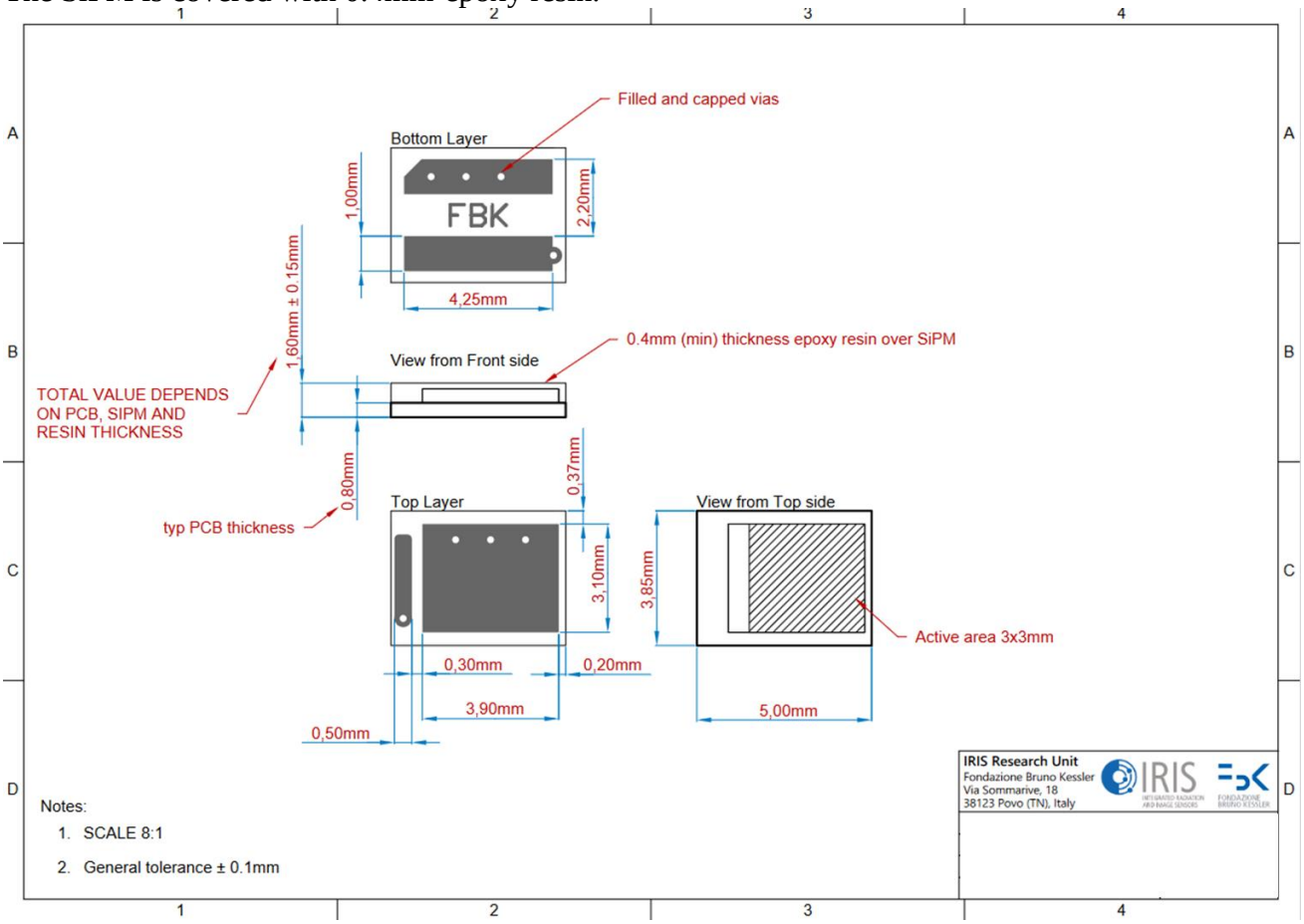
Safe solutions must be adopted for the handling and shipment.



Example project 2

Packaging of 3x3mm SiPM mounted with surface mounting technique (SMT) on a PCB 5mmx3.65mm. The front side pad of SiPM is wire bonded on the PCB, whereas the back contact of the SiPMis glued to the PCB with conductive resin. The 2 PCB pads are connected through vias to the bottom side of the PCB.

The SiPM is covered with 0.4mm-epoxy resin.

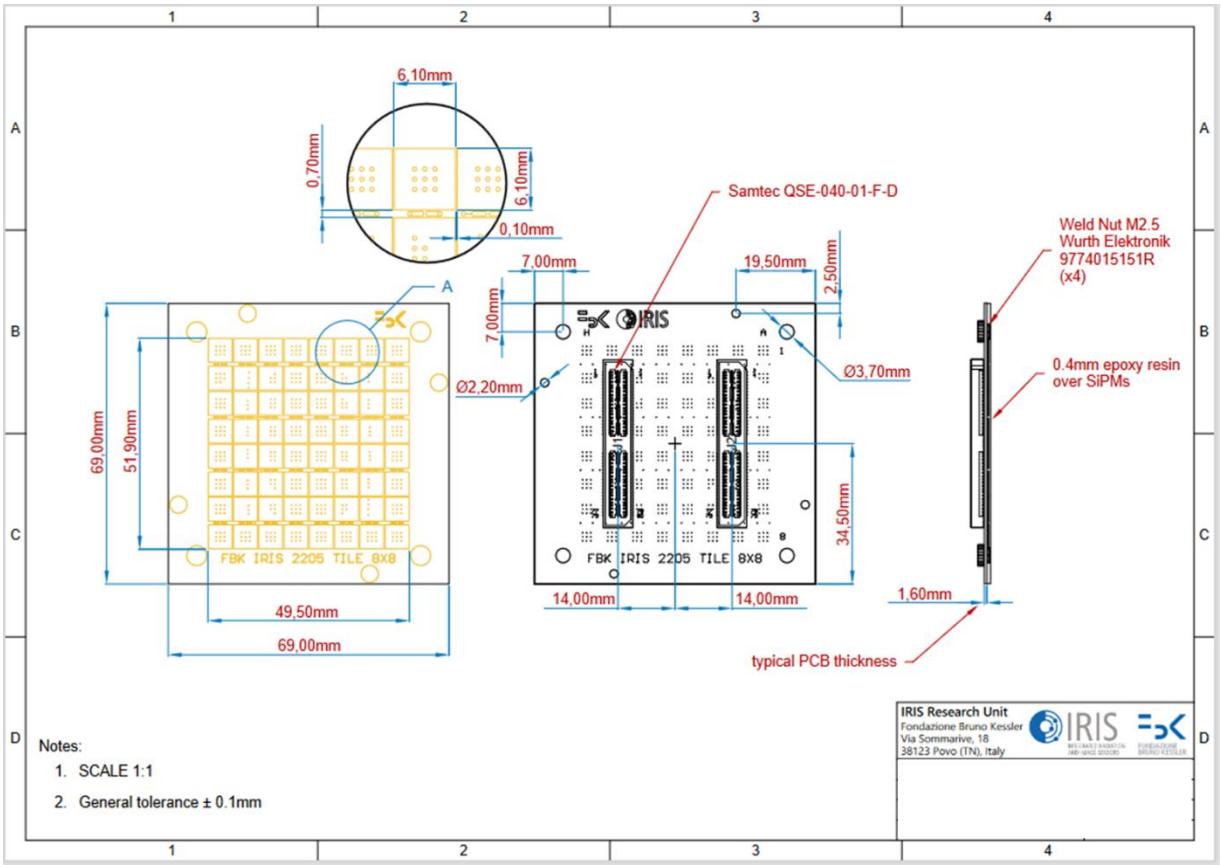


Example project 3

Production of 8x8 channels tiles with 6x6mm SiPMs. The SiPM are glued with conductive resin on the PCB to electrically connect their backside electrods, the front side pads of SiPMs are wire bonded on corresponding pads on the PCB (FR4 halogen free, 1.6mm thickness). The spacing between SiPM dies is 0.1mm, except for the side assigned to the wire bonding where the spacing is bigger (0.7mm).

SAMTEC connectors are used to access the bias and readout channels of the tile.

No optical resin is used to encapsulate the tile, the handling is guaranteed by using weld nuts M2.5.



CONNECTORS PINOUT TABLE

·CONNECTOR 1

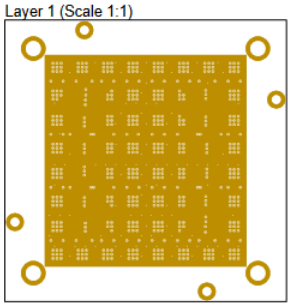
CONNECTOR PIN No.	CHANNEL No.	CONNECTOR PIN No.	CHANNEL No.
1	K(G-1)	2	K(F-1)
3	K(H-1)	4	K(E-1)
5	*NC*	6	*NC*
7	A(G-1)	8	A(F-1)
9	A(H-1)	10	A(E-1)
11	A(H-2)	12	A(E-2)
13	A(G-2)	14	A(F-2)
15	*NC*	16	*NC*
17	K(H-2)	18	K(E-2)
19	K(G-2)	20	K(F-2)
21	K(G-3)	22	K(F-3)
23	K(H-3)	24	K(E-3)
25	*NC*	26	*NC*
27	A(G-3)	28	A(F-3)
29	A(H-3)	30	A(E-3)
31	A(H-4)	32	A(E-4)
33	A(G-4)	34	A(F-4)
35	*NC*	36	*NC*
37	K(H-4)	38	K(E-4)
39	K(G-4)	40	K(F-4)
41	K(G-5)	42	K(F-5)
43	K(H-5)	44	K(E-5)
45	*NC*	46	*NC*
47	A(G-5)	48	A(F-5)
49	A(H-5)	50	A(E-5)
51	A(H-6)	52	A(E-6)
53	A(G-6)	54	A(F-6)
55	*NC*	56	*NC*
57	K(H-6)	58	K(E-6)
59	K(G-6)	60	K(F-6)
61	K(G-7)	62	K(F-7)
63	K(H-7)	64	K(E-7)
65	*NC*	66	*NC*
67	A(G-7)	68	A(F-7)
69	A(H-7)	70	A(E-7)
71	A(H-8)	72	A(E-8)
73	A(G-8)	74	A(F-8)
75	*NC*	76	*NC*
77	K(H-8)	78	K(E-8)
79	K(G-8)	80	K(F-8)

·CONNECTOR 2

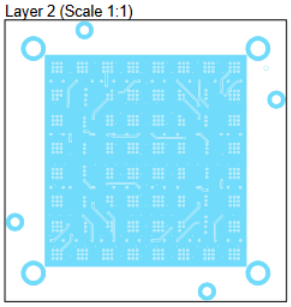
CONNECTOR PIN No.	CHANNEL No.	CONNECTOR PIN No.	CHANNEL No.
1	K(C-1)	2	K(B-1)
3	K(D-1)	4	K(A-1)
5	*NC*	6	*NC*
7	A(C-1)	8	A(B-1)
9	A(D-1)	10	A(A-1)
11	A(D-2)	12	A(A-2)
13	A(C-2)	14	A(B-2)
15	*NC*	16	*NC*
17	K(D-2)	18	K(A-2)
19	K(C-2)	20	K(B-2)
21	K(C-3)	22	K(B-3)
23	K(D-3)	24	K(A-3)
25	*NC*	26	*NC*
27	A(C-3)	28	A(B-3)
29	A(D-3)	30	A(A-3)
31	A(D-4)	32	A(A-4)
33	A(C-4)	34	A(B-4)
35	*NC*	36	*NC*
37	K(D-4)	38	K(A-4)
39	K(C-4)	40	K(B-4)
41	K(C-5)	42	K(B-5)
43	K(D-5)	44	K(A-5)
45	*NC*	46	*NC*
47	A(C-5)	48	A(B-5)
49	A(D-5)	50	A(A-5)
51	A(D-6)	52	A(A-6)
53	A(C-6)	54	A(B-6)
55	*NC*	56	*NC*
57	K(D-6)	58	K(A-6)
59	K(C-6)	60	K(B-6)
61	K(C-7)	62	K(B-7)
63	K(D-7)	64	K(A-7)
65	*NC*	66	*NC*
67	A(C-7)	68	A(B-7)
69	A(D-7)	70	A(A-7)
71	A(D-8)	72	A(A-8)
73	A(C-8)	74	A(B-8)
75	*NC*	76	*NC*
77	K(D-8)	78	K(A-8)
79	K(C-8)	80	K(B-8)

Copper pours connected to GND pins of the connector QSE-040-01-F-D

Layer 1 (Scale 1:1)



Layer 2 (Scale 1:1)



Bottom Layer (Scale 1:1)